IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number: 7,112,504

Serial No.: 10/694,684

Issued: September 26, 2006

Inventor(s): Ping-Yi Hsin et al.

Title: METHOD OF FORMING METAL-INSULATOR-METAL (MIM) CAPACITORS AT COPPER PROCESS

Attention Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PTO MISTAKE (37 CFR 1.322)

Dear Sir:

1. Attached is Form PTO/SB/44 wherein the errors occurring in the printed patent are noted by column and line number.

2. The exact page and line number where the correct language appears in the application file is:

Declaration filed with application on 10/28/2003 and second inventor's name in Official Filing Receipt dated 5/3/2004;

Application Abstract filed 10/28/2003, page 22;

Amendment as filed 8/29/2005, page 2; and

Application as filed 10/28/2003, page 13, line 1.

3. Please send the Certificate to:

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Respectfully submitted,

Date: JUNE 29, 2007

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,112,504

APPLICATION NO.: 10/694,684

ISSUE DATE : September 26, 2006

INVENTOR(S) : Ping-Yi Hsin and Zin Chein Wei

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(75) Inventors: delete "Zan Chun Wei" and insert therefore - - Zin Chein Wei - - .

ABSTRACT delete entire abstract and insert:

- - A method of forming a MIM capacitor, and the resultant MIM capacitor, comprising the following steps. A structure having a metal structure formed thereover is provided. A dielectric layer is formed over the metal structure and a top layer is formed over the dielectric layer. A capacitance trench is formed through the top layer and into the dielectric layer. Respective bottom electrodes are formed over the opposing side walls of the capacitance trench. A capacitance dielectric layer is formed over: the respective bottom electrodes; the bottom of the capacitance trench; and the remaining top layer. Respective opposing initial via openings are formed adjacent the capacitance trench. Respective trench openings are formed above, continuous and contiguous with the lower portions of the respective opposing initial via openings and exposing portions of the underlying metal structure to form respective opposing dual damascene openings. Planarized metal portions are formed within: the dual damascene openings; and the capacitance trench to form a top electrode. - -

Column 4, line 19, after "16" insert - - are etched - -.

Column 4, line 25, after "12" insert - - and bottom electrodes 30', 30". Capacitance trench 25 includes sidewalls 50 formed of remaining portions of capacitance dielectric layer 32". - -

Column 4, line 57, delete "Prestent" and insert therefore - - Present - -.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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